IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application for:	Examiner: Garcia, J.
Pooi See Lee	Group Art Unit: 2823
Serial No.: 09/726,903	
Filing Date: 11/29/2000	
For: METHOD AND APPARATUS FOR PERFORMING NICKEL SALICIDATION	

AMENDED APPEAL BRIEF

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This amended appeal brief is filed in response to the 07/09/2004 Notification of Non-Compliance with the Requirements of 37 CFR 1.192(c).

This is an Appeal from the final rejection of claims 1-15 in the above-referenced application. In accordance with 37 C.F.R. § 1.192, this Brief, along with the accompanying Appendices, is filed in triplicate. Appellant previously paid the required fee. Please charge any additional fees or credit any overpayment to Deposit Account No. 501128, referencing CHAR.P0003.

I. REAL PARTY IN INTEREST

The real party in interest to this Appeal is Chartered Semiconductor Ltd, a corporation of the republic of Singapore, having its principal place of business in Singapore.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignees thereof.

III. STATUS OF CLAIMS

Claims 1-15 are pending in the present application. The examiner has rejected claims 1-15. Applicant hereby appeals the rejection of claims 1-15.

IV. STATUS OF AMENDMENTS

A proposed amendment was filed subsequent to final rejection. The examiner acted upon the proposed amendment. The proposed amendment was denied entry. An Advisory Action to that effect was mailed December 24, 2003.

V. SUMMARY OF INVENTION

A nickel salicide process may be used to form low resistivity gate electrodes and source/drain contacts. (*Specification*, page 6, lines 2-3). A processed substrate is formed by fabricating integrated circuit components on a silicon substrate. In one embodiment, the procedure for forming the processed substrate includes forming dielectric regions in the silicon substrate that electrically isolate neighboring integrated circuit devices, doping portions of the silicon to form source/drain structures, depositing a gate dielectric material and a polycrystalline silicon gate material onto the silicon substrate and selectively etching, and depositing a dielectric material onto the silicon substrate and selectively etching to form dielectric spacers. (*Specification*, page 6, lines 10-17).

After forming the processed substrate, nitrogen is incorporated. In one

embodiment, the nitrogen is introduced by ion implantation. (*Specification*, page 6, lines 17-20). After incorporation of the nitrogen, the processed substrate is annealed to reduce implantation defects. Thereafter, nickel is deposited on the processed substrate and subsequently annealed. During sample annealing, nickel reacts with silicon to form nickel mono-silicide. (*Specification*, page 6, lines 20-23).

VI. ISSUES

Whether the subject claims are anticipated, under 35 U.S.C. §102(e), by Miura, et al. (U.S. Patent 6,346,465, hereinafter referred to as "*Miura et al.*")?

VII. GROUPING OF THE CLAIMS

Applicants contend that all of the pending claims (1-15) stand or fall together. Accordingly, Applicants are not grouping the claims on appeal.

VIII. ARGUMENT

A. TO ANTICIPATE A CLAIM, A REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). "The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, *i.e.*, identity of terminology is not required." *In re Bond*, 910 F.2d 831,

15 USPQ2d 1566 (Fed. Cir. 1990). *MPEP 2131.*

B. MIURA ET AL. DO NOT TEACH ALL THE ELEMENTS OF THE CLAIMED INVENTION.

1. Claim 1 Includes An Annealing Step After Nitrogen Incorporation and Before Nickel Deposition.

Claim 1 includes the following recitations:

incorporating nitrogen into said processed substrate;
annealing said processed substrate after incorporating nitrogen into said processed substrate for removing defects caused by nitrogen implantation;
depositing nickel onto said processed substrate

As claimed, the subject method invention requires an annealing step subsequent to nitrogen implantation and prior to nickel deposition.

2. *Miura et al.* Do Not Disclose An Annealing Step After Nitrogen Incorporation and Before Nickel Deposition

The Examiner points to Column 8, lines 56-61 as disclosing the element of "incorporating nitrogen into at least a region smaller than the entire top surface of the processed substrate and annealing the processed substrate." *Miura et al.* discuss the direct nitridation of a substrate in an ammonia atmosphere at 300 °C in the subject section. However, *Miura et al.* do not mention a separate annealing step. *Miura et al.'s* disclosure of the nitridation process occurring at 300 °C is not equivalent to the claimed "annealing" process. As claimed in claim 1, the annealing process is performed to remove defects of the process (*i.e.*, "removing defects caused by nitrogen implantation"). With regard to this

annealing step, the Specification discloses:

> In some embodiments, rapid thermal processing at a temperature between 800°C and 1000°C, for a duration of between 30 seconds and 60 seconds, removes implantation defects with very little "drive-in diffusion" of nitrogen. (*Specification*, page 11, lines 19 – 22).

Applicants respectfully contend that *Miura et al.* do not anticipate the claimed invention because *Miura et al.* do not teach annealing the substrate after incorporating the nitrogen and before the nickel deposition process.

3. The 35 U.S.C. § 102 Rejection Should Be Withdrawn

As *Miura et al.* do not disclose all elements of claim 1, which is the only independent claim at issue, Applicants respectfully request that the anticipation rejection be withdrawn.

C. NO GROUNDS OF REJECTION HAVE BEEN STATED FOR CLAIMS 4-7.

No grounds for the rejection of claims 4-7 is stated in the Final Office Action mailed 08/27/2003. Applicants respectfully request clarification on this issue.

///

IX. CONCLUSION.

In view of the foregoing, applicants respectfully submit that the claims are patentable. Applicants hereby request that the Board overturn the examiner's finding that the claims are unpatentable under 35 U.S.C. §102(e).

BY: _____

Vincent Tassinari
Reg. No. 42,179
Date: September 2, 2004
Tel. No.: 650.752.0990 ext. 100

APPENDIX

The following claims are the subject of this Appeal.

1. (Previously Amended) A method of nickel salicidation comprising:

forming a processed substrate including partially fabricated integrated circuit components and a silicon substrate;

incorporating nitrogen into said processed substrate;

annealing said processed substrate after incorporating nitrogen into said processed substrate for removing defects caused by nitrogen implantation;

depositing nickel onto said processed substrate; and

annealing said processed substrate so as to form nickel mono-silicide.

2. (Original) The method as claimed in claim 1, wherein said partially fabricated integrated circuit components include gate and source/drain structures.

3. (Previously Amended) The method as claimed in claim 2, wherein said forming a processed substrate comprises:

forming dielectric regions in said silicon substrate that electrically isolate neighboring integrated circuit devices;

doping a portion of said silicon substrate with an n-type and p-type doping to form said source/drain structures;

depositing a gate dielectric material and a polycrystalline silicon gate material onto said silicon substrate and selectively etching; and

depositing a dielectric material onto said silicon substrate and selectively etching to form dielectric spacers.

4. (Original) The method as claimed in claim 1, wherein said incorporating nitrogen into said processed substrate comprises doping said processed substrate with nitrogen.

5. (Original) The method as claimed in claim 1, wherein said incorporating nitrogen into said processed substrate comprises implanting nitrogen ions into said processed substrate.

6. (Original) The method as claimed in claim 5, wherein said implanting nitrogen ions comprises a blanket N_2+ ion implantation of said processed substrate.

7. (Original) The method as claimed in claim 6, wherein said blanket N_2+ ion implantation comprises implanting ions with a dosage between $2*10^{14}/cm^2$ and $2*10^{16}/cm^2$, and an ion energy between 15 keV and 50 keV.

8. (Original) The method of claim 1, further comprising annealing said processed substrate prior to said depositing nickel.

9. (Original) The method as claimed in claim 8, wherein said annealing said processed substrate prior to said depositing nickel comprises rapid thermal

processing at a temperature between 800 °C and 1000 °C, for a duration of between 30 seconds and 60 seconds.

10. (Original) The method as claimed in claim 1, wherein said depositing nickel comprises applying a solution including hydrogen fluoride to said processed substrate and blanket sputter depositing between 100 Å and 300 Å of said nickel onto said processed substrate.

11. (Original) The method as claimed in claim 1, wherein said annealing said processed substrate so as to form nickel mono-silicide comprises one-step rapid thermal processing at a temperature between 400 °C and 800 °C.

12. (Original) The method as claimed in claim 1, further comprising:

removing unreacted nickel after said annealing said processed substrate so as to form nickel mono-silicide; and

performing a series of integrated circuit fabrication procedures after said removing unreacted nickel, including:

depositing a dielectric material onto said processed substrate and selectively etching;

planarizing said processed substrate; and

depositing metal onto said processed substrate and selectively etching to form metal lines.

13. (Original) The method as claimed in claim 12, wherein said removing unreacted nickel comprises etching said unreacted nickel using a solution containing at least one of sulfuric acid, hydrogen peroxide, nitric acid, hydrochloric acid, water, a solution of sulfuric acid, hydrogen peroxide and water, a solution of nitric acid and hydrochloric acid, and a solution of hydrochloric acid, hydrogen peroxide and water.

14. (Original) The method as claimed in claim 12, wherein said annealing said processed substrate so as to form nickel mono-silicide and said removing unreacted nickel comprise a process to form a gate electrode including nickel mono-silicide and polycrystalline silicon that is electrically isolated from a source/drain contact including nickel mono-silicide and single crystal silicon.

15. (Original) The method as claimed in claim 1, wherein at least one of said incorporating nitrogen and said depositing nickel is applied to a region smaller than the entire top surface of the processed substrate.

Claims 16-24 (previously canceled)